Fault-Tolerant Control of Current Measurement Circuits for Three-Phase Grid-Connected Inverters

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Abstract: Three-phase grid-connected inverters (GCIs) are essential components in distributed generation systems, where the accuracy of current measurement circuits is fundamental for reliable closed-loop operation. Nevertheless, the presence of a DC offset in the measured current can disrupt the regulation of grid currents and significantly degrade system performance. In this work, a fault-tolerant control approach is introduced to counteract the impact of such offset faults through a dedicated current compensation mechanism. The proposed solution is built around two main stages: (i) detecting and isolating DC offset faults that may appear in one or multiple phases of the measured grid currents, and (ii) estimating the fault magnitude and reconstructing the corrected current signal. The offset magnitude is obtained analytically by examining the grid current projected onto the synchronous d-axis at the grid angular frequency, eliminating the need for any additional sensing hardware. Simulation and experimental investigations conducted under several fault scenarios confirm the robustness of the proposed strategy and highlight significant improvements in detection speed and diagnostic accuracy.

Keywords: fault detection Grid connected inverter; fault tolerant control; fault isolation; sensing circuit

I. Introduction

With the steady rise in global electricity demand, renewable-based distributed generation has become increasingly prominent in modern power systems. Grid-connected inverters (GCIs) constitute the essential interface between these distributed energy resources and the utility grid. Among the various GCI architectures, Cascaded H-Bridge Multilevel Inverters (CHBMLIs) are particularly attractive thanks to their modular design, ability to produce high-quality output waveforms, and lower switching losses. These advantages make CHBMLI solutions highly suitable for applications involving photovoltaic and wind energy sources [1]. GCIs are generally exposed to two broad categories of faults: electrical faults and measurement-related faults. Electrical faults often arise from open-circuit or short-circuit failures in power semiconductor switches [2]. While short-circuit issues are commonly handled through dedicated hardware protection circuits, the majority of recent studies have concentrated on diagnosing and mitigating open-circuit failures [3–6].

In parallel, Measurement Circuits (MCs) are crucial for supplying accurate real-time feedback to the control system, and any degradation in measurement quality can significantly affect overall inverter performance [7]. For this reason, the present work focuses on fault-tolerant control in the presence of single-phase or dual-phase Current Measurement

Faults (CMFs). Ensuring reliable operation under such conditions requires precise fault identification and the deployment of an appropriate Fault-Tolerant Control (FTC) mechanism.

An effective Fault-Tolerant Control (FTC) scheme relies on accurate fault diagnosis, since an incorrect assessment may trigger an inappropriate control action and potentially cause additional system failures. Existing approaches for fault detection and identification are generally grouped into three main classes: model-based methods [8], signal-based methods [9], and data-driven methods [10]. Compared to the first two categories, data-driven approaches offer superior adaptability and robustness, particularly when dealing with systems exhibiting complex or nonlinear behaviors [10–14]. These methods also avoid the need for an accurate analytical model; instead, they exploit historical fault data to establish relationships between observed fault signatures and their corresponding categories.

Within data-driven diagnostic frameworks, various signal-processing and feature-extraction techniques are used to enhance distinguishable fault characteristics. For example, the works in [10, 11] employ Fourier and Wavelet transforms to analyze raw signals. While the Fourier transform provides a clear representation of frequency components, it disregards temporal information. Conversely, the Wavelet transform offers a joint time–frequency representation, enabling a more detailed and informative characterization of fault-related patterns [12].

To extract meaningful fault-related characteristics, the study in [13] applies principal component analysis to identify voltage fault signatures in the frequency domain, while [14] employs the ReliefF algorithm to select the most informative features. These two approaches address complementary objectives: the former prioritizes retaining the maximum amount of signal information during feature extraction, whereas the latter emphasizes improving the discriminative power of the selected features for classification tasks.

Most data-driven diagnosis frameworks depend on predefined monitoring variables. Although substantial research has focused on extracting and processing fault features, comparatively less attention has been given to determining which monitoring signals are most effective. In [15], a genetic algorithm is used to select the optimal fault-relevant variables for each fault type, with a principal component analysis model built for each chosen subset. Reference [16] introduces several cost functions that quantify the contribution and discriminative capability of original signals for various faults. Additionally, [17] adopts a maximum relevance–minimum redundancy criterion within a distributed structure to identify the most informative variables for each subsystem. These techniques share the goal of evaluating and selecting monitoring signals that enhance diagnostic performance through well-defined assessment metrics.

Such methods are commonly applied in large-scale dynamic systems where establishing accurate mathematical models is difficult. Even though a mathematical representation of a grid-connected inverter can be formulated, determining exact parameter values remains challenging in practice. For these systems, the selection of monitoring signals is often based on the correlation between candidate variables and the target diagnostic indicators [17–19]. When a detailed and reliable model, such as that of a grid-connected inverter, is available, it becomes important to introduce new strategies for identifying the most appropriate monitoring signals.

In recent years, numerous fault-tolerant control (FTC) schemes have been proposed for power converters, particularly to address current sensor malfunctions [18–21]. These methods generally fall into two major categories: observer-based approaches and signal compensation techniques. Observer-based structures offer fast fault detection and rapid control reconfiguration. For example, [18] estimates angular velocity and constructs a stator flux observer to isolate sensor faults in motor drives, thus maintaining continuous operation. Likewise, [19] develops multiple observers capable of detecting and handling one or two faulty sensors in motor drive systems. However, these observer-dependent techniques typically require accurate system models, which becomes increasingly difficult for complex converter architectures such as Cascaded H-Bridge Multilevel Inverters CHBMLIs, due to their modular structure, numerous switching devices, and nonlinear dynamics.

To reduce the dependence on accurate mathematical models, signal compensation–based solutions have attracted increasing attention, especially for CHBMLI architectures. These approaches attempt to reconstruct faulty measurements directly from available signals, avoiding the need for detailed system modeling. For instance, [20] proposes a model-independent compensator capable of correcting sensor inaccuracies while maintaining a low computational load. In a similar direction, [21] restores faulty current measurements by exploiting information from the remaining healthy phases. Although such techniques show promising results, they are often developed for motor-drive applications and are generally restricted to scenarios involving only one or two faulty sensors. Furthermore, the

influence of the closed-loop control dynamics on the fault signatures is frequently overlooked, which can degrade the reliability of the diagnostic process.

Beyond model-based and signal-level methods, data-driven diagnostic techniques have also been investigated. These methods rely heavily on the in formativeness of the diagnostic signals. Current measurements, however, are highly sensitive to variations in load conditions, which may hinder fault discrimination [13]. To address this issue, some works instead utilize inverter output voltage as the diagnostic variable [22]. Nonetheless, the characteristics of voltage-based faults are strongly shaped by the current control loop under grid-connected operation, potentially reducing detestability [23]. Advanced control strategies have therefore been introduced to improve the dynamic behavior of grid-connected converters [24–26], generally formulated in either the synchronous dq frame or the stationary αβ frame [27, 28]. Since both transformations depend on the currents measured by the sensing circuit, any measurement fault may distort the transformed quantities, diminish fault-related features, and negatively impact diagnostic performance.

A recent work in [29] presents an observer-based FTC approach dedicated to detecting and compensating multiple current-sensor offset faults in grid-connected inverters. The method is implemented in the αβ frame and relies on an auxiliary current sensor to support fault estimation and ensure proper control reconfiguration. While effective, this strategy requires accurate system modeling and additional hardware, which can limit applicability in modular converter structures and increase implementation cost. In contrast, the method developed in this paper is entirely model-free and does not require supplementary sensors. The proposed scheme analytically estimates the magnitude of current offset faults through frequency-domain evaluation of the direct-axis current component in the synchronous dq frame, making it particularly well suited to CHBMLI-based grid-connected systems.

This work introduces a novel fault-tolerant control (FTC) strategy aimed at compensating offset faults occurring in the three-phase current measurement circuits of grid-connected inverters. The approach does not rely on parameter knowledge or extra instrumentation. By applying frequency-domain analysis to the d-axis current, a residual-driven detection mechanism is formulated, enabling precise fault identification and rapid signal correction. Consequently, stable closed-loop performance is maintained even under faulty measurement conditions.

The main contributions of this work can be summarized as follows. First, a fully model-free fault detection and compensation approach is developed to address DC offset faults affecting current sensors in three-phase grid-connected CHBMLI systems. The proposed method enables an analytical estimation of the fault magnitude directly in the synchronous reference frame, eliminating the need for observers or additional sensing hardware. Areal-time compensation mechanism is then implemented to reconstruct the corrupted current measurements, ensuring continuous and stable operation of the closed-loop control system. Moreover, the technique is capable of managing both single-phase and dual-phase sensor faults while maintaining robustness against variations in system parameters. The remainder of the paper is organized as follows: Section 2 introduces the problem formulation, Section 3 details the proposed Fault Detection and Isolation (FDI) scheme and the offset compensation strategy for the current measurement circuit, Section 4 presents simulation and experimental results, Section 5 provides an analysis and discussion of the limitations of the proposed FTC approach, and Section 6 concludes the paper.

II. Problem Description

Figure 1(a) presents the block diagram of a three-phase CHBMLI with voltage levels connected to the electrical grid. Each inverter leg is composed of nnn fundamental H-bridge modules. Utilizing grid information provided by the Phase-Locked Loop (PLL), the measured phase currents are transformed from the abc reference frame into either the synchronous dq frame or the stationary αβ frame to facilitate accurate control and reference tracking. The resulting current control outputs are used to generate the modulation voltage, which is then applied to the Carrier Phase Shifting Pulse Width Modulation (CPS-PWM) strategy to produce the PWM signals required for switching the inverter devices. The mathematical model of the inverter can be expressed as follows:

$$Ri_{abc} + L\frac{di_{abc}}{dt} + V_{gabc} = V_{abc} \qquad (1)$$

Here, L denotes the filter inductance, while R represents the corresponding series resistance. The term i_{abc} indicates the grid current, and V_{gabc} refers to the grid voltage measured at the point of common coupling

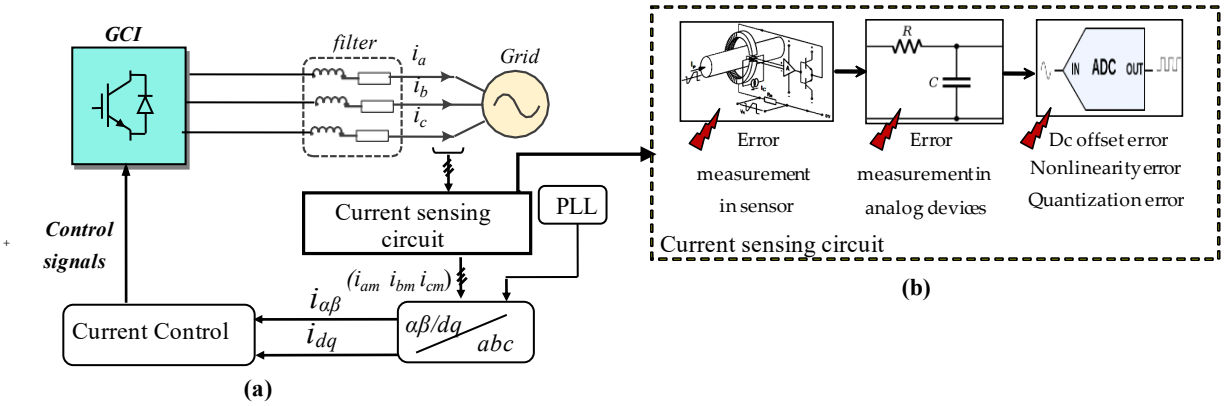

Figure 1. (a) Block diagram of a grid connected inverter **(b)** Error factors in current measurement circuit.

To illustrate the measurement process, consider a conventional PI-based current control loop in which the measured currents ideally coincide with the actual grid currents (i_a,i_b,i_c). These currents are acquired through the measurement chain shown in Figure 1(b), which typically consists of Hall-effect sensors, a signal conditioning stage, filtering circuits, and an ADC. Despite its widespread use, this measurement path is vulnerable to several types of errors, including scaling inaccuracies and DC offset faults. Such faults may originate from the sensing element, from non-ideal behaviors in analog circuitry, or from the ADC interface. For example, because the ADC input is referenced to ground through a grounding resistor, a fault can cause the sampled analog voltage to drift from its nominal level. Under healthy operating conditions, the grid currents can be expressed as shown in (2).

$$\begin{aligned} i_a(t) &= I_m \cos(\omega_g t) \\ i_b(t) &= I_m \cos(\omega_g t - \frac{2\pi}{3}) \\ i_c(t) &= I_m \cos(\omega_g t + \frac{2\pi}{3}) \end{aligned} \quad (2)$$

Where he term I_m denotes the peak value of the grid current. When a DC offset fault occurs in the current measurement stage, each sensor introduces a constant bias. This offset, denoted by D_{abc} [15], reflects the undesired deviation added to the actual current. Consequently, under an offset fault, the three-phase currents delivered by the measurement chain can be expressed as:

$$\begin{aligned} i_{am}(t) &= i_a(t) + D_a \\ i_{bm}(t) &= i_b(t) + D_b \\ i_{cm}(t) &= i_c(t) + D_c \end{aligned} \quad (3)$$

The influence of offset faults on the control system is analyzed in the synchronous dq reference frame. The measured currents transformed into this frame are expressed in (4). In this representation, the id and iq components exhibit distinct frequency characteristics: one corresponds to a DC term, while the other oscillates at the grid's angular frequency. These behaviors are summarized in (5) and further discussed in the following analysis.

$$\begin{bmatrix} i_d(t) \\ i_q(t) \end{bmatrix} = = \begin{bmatrix} i_{d,1}(t) + i_{d,2}(t) \\ i_{q,1}(t) + i_{q,2}(t) \end{bmatrix} \quad (4)$$

The d axis current is expressed as:

$$\begin{aligned} i_{d,1}(t) &= I_m \\ i_{d,2}(t) &= 2/3((D_a - D_c)cos(\omega_g t) + (D_b \\ &\quad - D_c)cos(\omega_g - 2\pi/3)) \end{aligned} \quad (5)$$

The q axis current is defined as:

$$\begin{aligned} i_{q,1}(t) &= 0 \\ i_{q,2}(t) &= -2/3((D_a - D_c)sin(\omega_g t) + (D_b \\ &\quad - D_c)sin(\omega_g t - 2\pi/3)) \end{aligned} \quad (6)$$

$i_{d,1}$ and $i_{q,1}$ are the dc components, while $i_{d,2}$ and $i_{q,2}$ are the AC ripple signals at ω_g.

As shown in (5) and (6), the d-axis current contains a DC component superimposed with ripple terms oscillating at the grid angular frequency. Conversely, the q-axis current is composed solely of these AC ripple components.

The frequency analysis along the d-axis current, illustrated in Figure 2, reveals the presence of a DC component and an AC component at 50 Hz when an offset fault occurs in the A-phase of the measurement circuit.

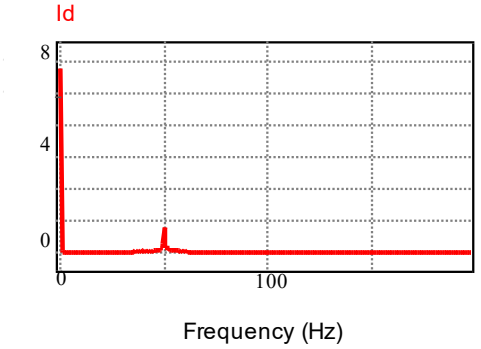

Figure 2 Frequency-domain response of the d-axis current under offset fault conditions.

III. Fault diagnosis and Compensation of Grid Current

The proposed strategy for detecting and compensating DC offset faults in the measured grid current is based on analyzing the d-axis current at the grid angular frequency ω_g. To isolate this component, the algorithm extracts id,2by applying a dedicated band-pass filter E(s), defined as follows:

$$E(s) = \frac{\omega_k s}{S^2 + \omega_k s + \omega_g^2} \quad (7)$$

Where ω_k represents the filter bandwidth. The center frequency of H(s) is ω_g.

This filter is purposefully designed to extract the oscillatory component at the grid fundamental frequency, which is directly influenced by DC offset faults. For reliable detection, ω_g is selected based on the nominal grid frequency , while the tuning parameter ω_k is set within 5% to 15% of ω_g. This choice S_1 provides a suitable compromise between noise attenuation and dynamic responsiveness. The performance of the filter was assessed under parameter variations and small frequency deviations ±1 Hz. The results confirm that it effectively isolates the desired component without introducing significant delay or distortion that could hinder accurate fault detection. Moreover, the band-pass filter maintains a second-order structure and remains stable for all positive values of ω_k, ensuring robustness and ease of implementation within the proposed approach.

A. Case 1: Single-Phase Offset Fault detection and compensation

The Fault Detection and Isolation procedure, together with the compensation for single-phase offset faults, is implemented by generating two residual signals, R_1 and R_2. The first residual, R_1, is obtained by computing the average of the products between $\cos(\omega_g t)$and $i_{d,2}(t)$, while the second residual, R_2, is calculated as the average of the products between $\cos\left(\omega_g t - \frac{2\pi}{3}\right)$ and $i_{d,2}(t)$. These residual signals are directly affected by the magnitudes of D_a, D_b and D_c, as detailed in equations (8), (9) and (10).

$$R_1 = <i_{d,2}(t)\cos(\omega_g t)>$$
$$R_2 = <i_{d,2}(t)\cos\left(\omega_g t - \frac{2\pi}{3}\right)> \quad (8)$$

Using orthogonality over one period:

$$<\cos(\theta)\cos(\theta)> = \frac{1}{2}$$
$$<\cos(\theta)\cos(\theta \pm {}^{2\pi}/_{3})> = -\frac{1}{4} \quad (9)$$

The residuals become:

$$\begin{cases} R_1 == \frac{1}{3}D_a - \frac{1}{6}D_b - \frac{1}{6}D_c \\ R_2 = \frac{1}{3}D_b - \frac{1}{6}D_a - \frac{1}{6}D_c \end{cases} \quad (10)$$

Under normal operating conditions, both residuals R_1 and R_2 remain at zero. The occurrence of a DC offset in any of the three-phase currents, however, induces deviations in these residuals, altering their magnitudes and signs. To determine which phase is affected, two Boolean fault indicators, F_1 and F_2, are defined as follows:

$$\begin{cases} F_{1,2} = 1 \quad if \quad R_{1,2} \geq 0 \\ F_{1,2} = 0 \quad if \quad R_{1,2} < 0 \end{cases} \quad (11)$$

To isolate the faulty measurement signal, a decision block, denoted as DB1 for single-phase offset faults, generates an alert signal S_1. When the current measurement circuit operates normally, both Boolean

indicators B_1 and B_2 are equal to one, yielding =0. If a DC offset is detected in phase A, F_1 remains 1 while F_2 becomes 0, resulting in S_1=1. In the case of a DC offset fault in phase b, F_1 is 0 and F_2 is 1, producing S_1=2. Finally, when the offset occurs in phase c, both F_1 and F_2 are 0, corresponding to S_1=3.

The undesirable ripple undulation in i_d brought on by the existence of DC offset in the current measurements has a significant impact on the current control loop. As a result, a method for compensation must be used in accordance with the residual (R_1 and/or R_2) values and S_1. Using this approach, the offset fault magnitude must be calculated and injected into the associated erroneous measurement. The compensated quantities, C_1, C_2 and C_3, correspond to the respective phases a, b and c when a DC offset fault occurs in the current sensing circuit are presented in equation (12).

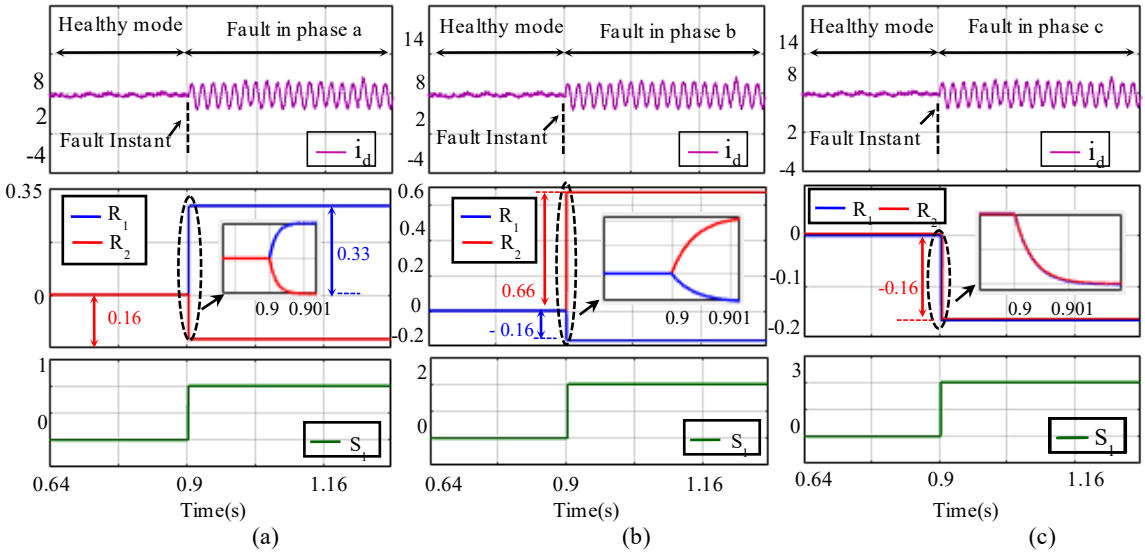

Figure 3 FDI of Single-phase offset fault : **(a)** DC offset in phase a. **(b)** DC offset in phase b. **(c)** DC offset in phase c.

$$\begin{cases} C_1 = -3R_1 \ , \ R_1 = \dfrac{1}{3}D_a \\ C_2 = 6R_1 \ , \ R_1 = -\dfrac{1}{6}D_b \\ C_3 = 6R_1 \ , \quad R_1 = -\dfrac{1}{6}D_c \end{cases} \tag{12}$$

Specifically, for the case where a DC offset fault is introduced in phase a, the grid current measurement is restored to its accurate value at the instant of fault appearance (t_f), as expressed in (13).

$$i_a(t_f) = \ i_{am}(t_f) + D_a \tag{13}$$

A comparable study was performed to examine the impact of a DC offset fault on the b and c phases of the measured grid current.

To assess the performance of the proposed FDI and compensation strategy for single-phase offset faults, simulation tests were carried out with the fault introduced at 0.9 s. In this case, a 1 A DC offset was applied individually to each phase of the current sensing circuit. As illustrated in Figure 3, the d-axis component of the grid current exhibits waveform distortion whenever a DC offset occurs in any of the phases.

Under healthy operating conditions, both residual signals R_1 and R_2 remain equal to zero. In this situation, no abnormal oscillations are detected, and the resulting Boolean indicators F_1 and F_2 stay at zero, keeping the offset alarm S_1 inactive. When an offset fault is introduced in the a-phase (Figure 3(a)), the residuals react accordingly: R_1 rises to approximately 0.33, whereas R_2 drops to around –0.16. According to (10), this configuration produces B_1 = 1 and B_2 = 0, which activates the alarm signal (S_1 = 1), confirming the presence of a DC offset in the a-phase current.

When the offset fault affects another phase, such as phase b or phase c, the residual pattern evolves differently, as described by (11). In the case of a b-phase offset, R_1 becomes negative (about –0.16) while R_2 becomes positive (near 0.66), which is the reverse trend observed for a-phase fault. For a c-phase fault, both residuals shift to negative values (approximately 0.16). Consequently, the alarm signal is set to S_1 = 2

for a b-phase fault and $S_1 = 3$ for a c-phase fault, as illustrated in Figures 3(b) and 3(c).
Offset compensation is performed by injecting a corrective term, calculated from the corresponding residual, into the affected current measurement. For an a-phase fault, the measured current i_{am} is corrected by adding the compensation term $C_1 = -3R_1$. Initially, the d-axis current exhibits ripple disturbances due to the offset error. Once the compensation is applied, these oscillations disappear and id rapidly returns to its nominal value within approximately 1.9 ms, as shown in Figure 4.

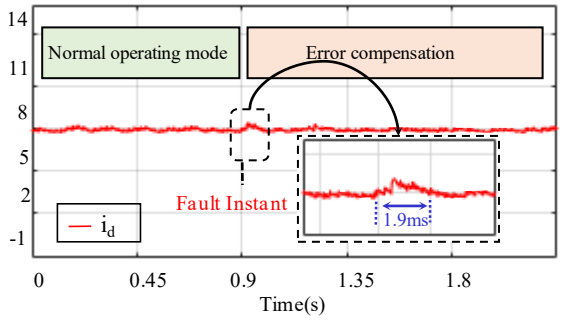

Figure 4 Offset fault compensation.

B. Case 1: Two-Phase Offset Fault Detection and Compensation

For two-phase offset faults, precise identification of faults affecting phase pairs such as (a, b), (a, c), or (b, c) requires the computation of three additional residuals, R_3, R_4 and R_5, which are constructed from the primary residuals R_1 and R_2. Each of these residuals targets a specific fault combination: R3 is associated with faults in phases (a, b), R_4 isolates faults in phases (a, c), and R_5 corresponds to faults in phases (b, c). Furthermore, examining the collective behavior of all residuals (R_j, with $j=1...5$) enables clear discrimination between single-phase faults and double-phase faults.
The expressions for R_3, R_4, and R_5 are given in equations (14), (15), and (16), respectively.

$$R_3 = R_2 - R_1 = -0.5D_a + 0.5D_b \quad (14)$$
$$R_4 = 2R_1 - R_2 = 0.5D_a - 0.5D_c \quad (15)$$
$$R_5 = R_1 + 2R_2 = 0.5D_b - 0.5D_c \quad (16)$$

The detection of two-phase offset faults can be determined by three conditions, summarized in Table1.

Table 1 Summary of Two-Phase Offset Fault Detection Conditions

Condition	*Faulty phases*
$C1: R_3 \neq 0\ or\ (R_4 \neq 0\ and\ R_3)$	(a, b)
$C2: R_4 \neq 0\ or\ (R_4 = 0\ and\ R_5 \neq 0)$	(a, c)
$C3: R_5 \neq 0\ or\ (R_5 = 0\ and\ R_3 \neq 0)$	(b, c)

To identify the erroneous measurement signals in the case of double-phase offset faults, a dedicated decision module DB2 is employed to generate the alarm signal S_2 based on predefined fault conditions.
- When the C_1 is satisfied, indicating an offset fault in phases a and b, the alarm S_2 is assigned a value of 1.
- For C_2, corresponding to a fault affecting phases a and c, S_2 takes the value 2.
- Similarly, when C_3 is met, representing a fault in phases b and c, S_2 is set to 3.

Whenever $S_2 \neq 0$, this confirms the presence of a double-phase offset fault, triggering the compensation procedure. In this mode, the appropriate corrective signals are applied to the faulty phases.
For a fault in phases a and b, the residuals R_1 and R_2 (from equations (8) and (9)) are used to calculate the corresponding DC offset components. These values are then employed to compute the compensation signals $C_{a,1}$ and $C_{b,2}$, which are applied to the a-phase and b-phase currents, respectively, thereby restoring the measured currents to their accurate values.

$$C\,1: \begin{cases} C_{a,1} = -2R_2 - 6R_1 \\ C_{b,1} = -4R_2 - 2R_1 \end{cases} \quad (17)$$

In this situation, the measured grid currents i_a and i_b are immediately corrected to their true values at the moment the fault occurs (t_f), as described in (18).

$$\begin{cases} i_a(t_f) = C_{a,1} + i_{am}(t_f) \\ i_b(t_f) = C_{b,1} + i_{bm}(t_f) \end{cases} \quad (18)$$

When a double-phase offset fault is detected in phases (b, c) or (a, c), corresponding to conditions 2 and 3, the compensation signals $C_{abc,j}$ are computed following the same procedure, where j denotes the condition number. This method guarantees that the correct compensation is applied for each fault scenario, as presented in equation (19).

$$C\,2: \begin{cases} C_{a,2} = 2(R_2 - R_1) \\ C_{c,2} = 2R_1 + 4R_2 \end{cases}$$
$$C\,3: \begin{cases} C_{b,3} = 2(-R_2 + R_1) \\ C_{c,3} = 2(R_2 + 2R_1) \end{cases} \quad (19)$$

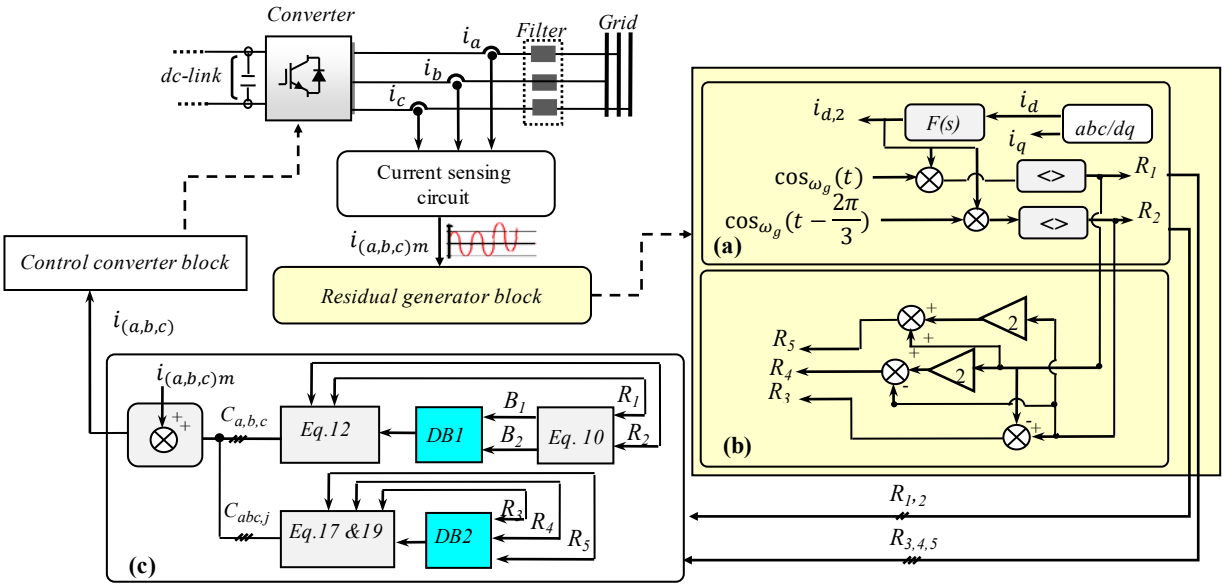

Figure 5 FTC of offset faults (a) R_1 and R_2 generation (b) R_3, R_4 and R_5 generation (c) Compensation block.

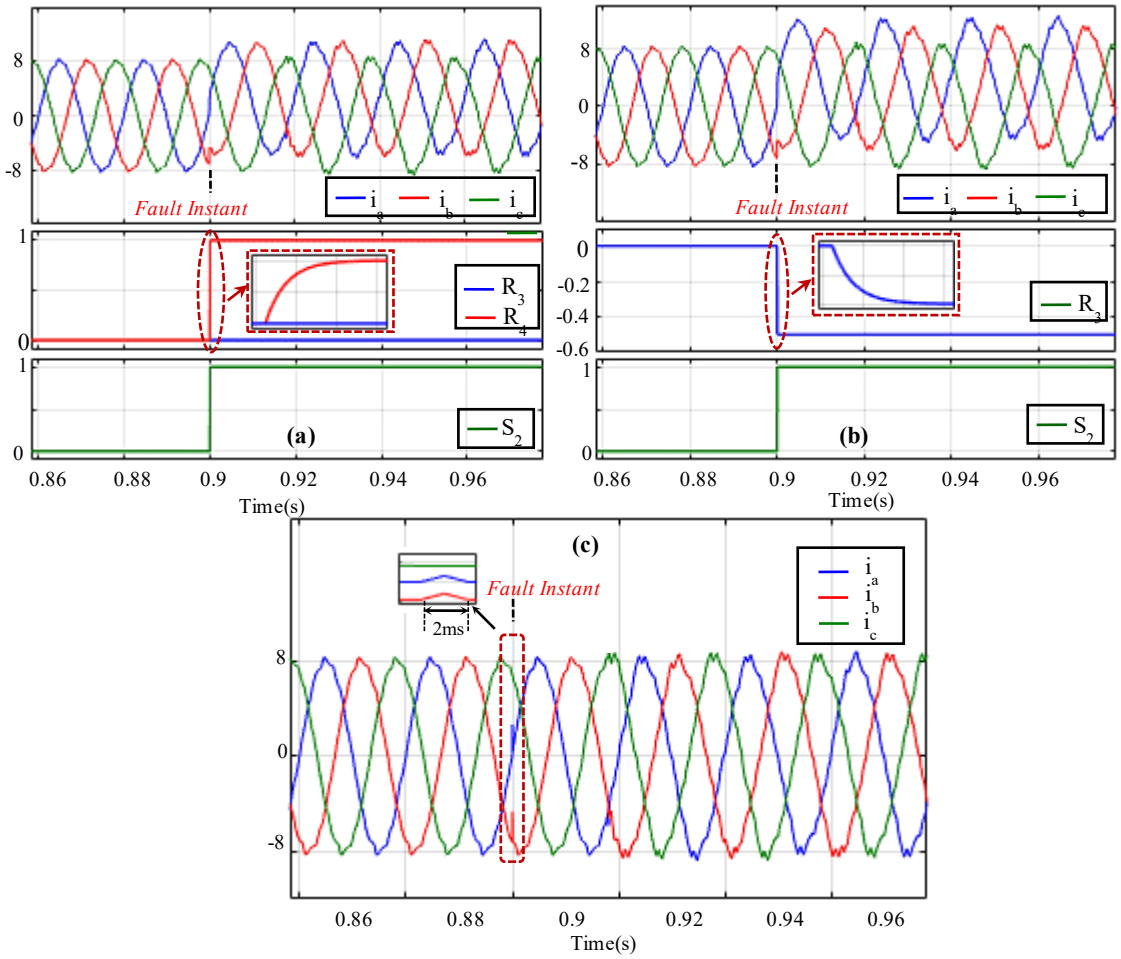

Figure 6 FDI of two-phase offset faults: (a) 2 A offset in phases (a, b), (b) 3 A offset in phase a and 2 A offset in phase b, (c) Compensation of the offset faults.

The block diagram for double-phase offset fault compensation is presented in Figure 5. The performance of the fault detection method for two-phase grid current faults is evaluated through two test scenarios involving phases a and b:

Scenario 1: A 2 A DC offset is applied simultaneously to phases a and b at 0.9 s (Figure 6(a)). After the fault occurs, residual R3 remains zero, requiring analysis of R4, which rises to +1 A. This change activates the alarm signal (S2 = 1), indicating faults in both phases.

Scenario 2: Different offset levels are applied to the two phases: 3 A in phase a and 2 A in phase **b** (Figure 6(b)). Here, residual R3 drops to –0.5 at the fault instant, correctly identifying faults in both phases.

The effectiveness of the compensation strategy is shown in Figure 6(c). For faults in phases a and b, the compensation terms $C_{a,1}$ and $C_{b,1}$ are added to the measured currents (i_{am} and i_{bm}), restoring them to their accurate values within 2 ms.

IV. Experimental Result and Discussion

The proposed method is validated using a three-phase grid-connected inverter test bench. The setup includes an STM32F4 controller, a DC power supply, an inverter, and an isolation transformer. Electrical quantities are measured with Hall-effect voltage and current sensors, an output filter, and analog conditioning circuits that adapt the signals for the digital platform. The STM32F4 generates the switching commands, which are sent to the inverter's gate drivers through a level-shifting interface. All signals are monitored in real time on a PC using the microcontroller's DAC module.

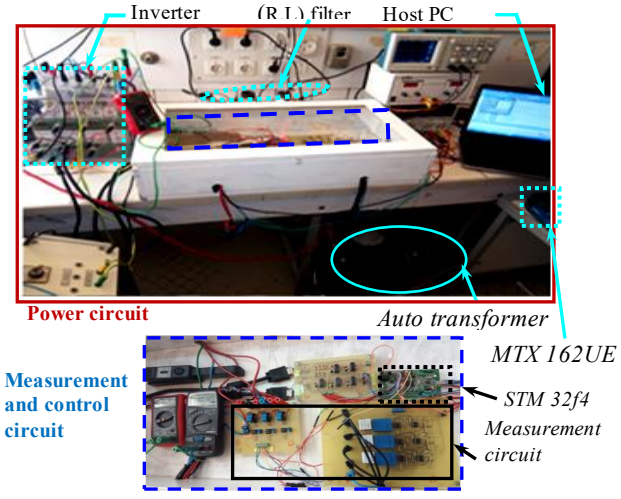

Figure 7 Experimental setup

Figure 8 illustrates the dynamic response of the three-phase inverter under a step change in the d-axis reference current. In Figure 8(a), the reference current (i_d^*) is increased from 8 A to 10 A at time tc, and the actual d-axis current (i_d) closely follows this change, achieving the new reference level within 2.8ms. This rapid tracking demonstrates the high responsiveness of the current control system.

Figure 8(b) depicts the tracking error between the reference and actual d-axis currents. When the reference is maintained at 8 A, the error is minimal, remaining below 0.38 A, indicating precise current regulation under steady-state conditions. Immediately following the step change, the error exhibits a transient peak due to the sudden reference change; however, the controller rapidly compensates for this disturbance, and the error quickly returns to a level below 0.38 A once the reference reaches 10 A. This behavior confirms the effectiveness of the control algorithm in minimizing overshoot and settling time.

Figure 8(c) shows the three-phase output current waveforms. It can be observed that all three-phase currents accurately track the reference change in the d-axis without introducing significant harmonic distortion or phase imbalance. The fast and precise response across all phases confirms the inverter's capability to maintain high-quality output currents, even under abrupt reference variations, which is essential for stable grid-connected operation. The effectiveness of the FDI and compensation algorithm is illustrated in Figure 9(a). An offset fault is introduced in the a-phase current at time t_1, creating an imbalance in the three-phase grid currents. At t_2, the proposed FTC method is activated, and the alarm signal S_1 rises to 1, indicating successful fault detection. The FTC action compensates the a-phase offset, and by t_3, the three-phase output currents return to a balanced state, allowing normal operation to resume within a short time. Figure 9(b) illustrates the experimental response of the system under a double-phase offset fault. At time t_1, DC offsets corresponding to 20% of the nominal current are simultaneously introduced in phases a and b, resulting in an observable imbalance in the three-phase grid currents. Upon activation of the proposed FTC algorithm at t_2, the system successfully identifies the presence of the faults in both phases and immediately applies the corresponding compensation signals. As a result, the measured currents in phases **a** and b are corrected, and by t_3, the three-phase output currents return to their balanced state within approximately 2 ms. This rapid correction confirms the effectiveness of the proposed method in simultaneously detecting and compensating multiple sensor faults, thereby maintaining stable and uninterrupted operation of the grid-connected inverter.

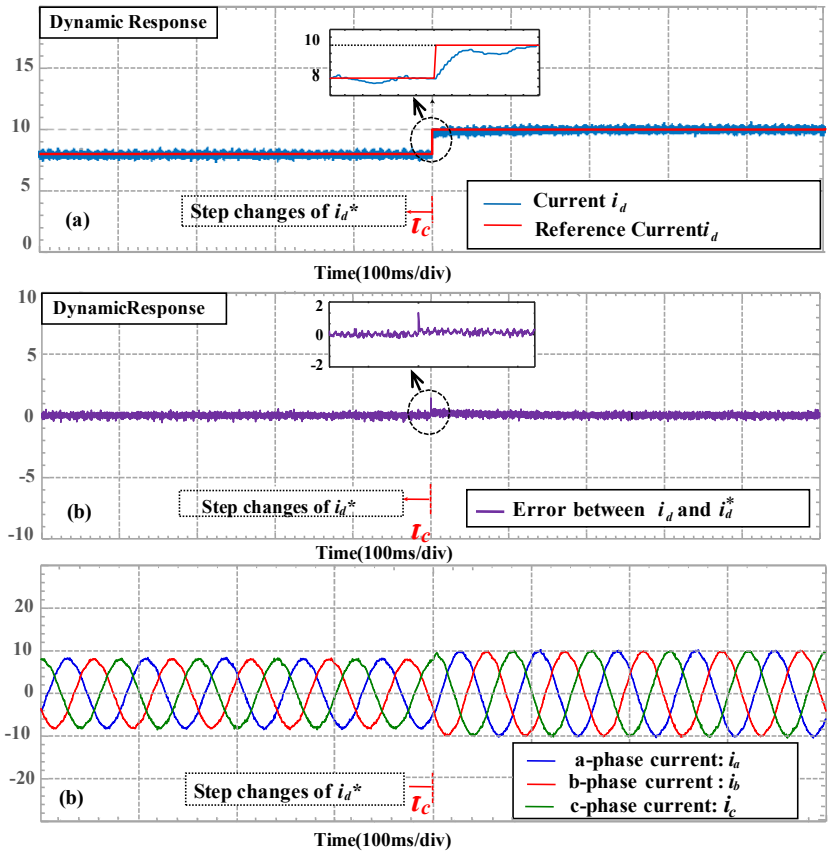

Figure 8 Experimental results of the system response: **(a)** Actual and reference grid current along the *d*-axis **(b)** Error between reference actual grid current along the *d*-axis **(c)** Three-phase grid current.

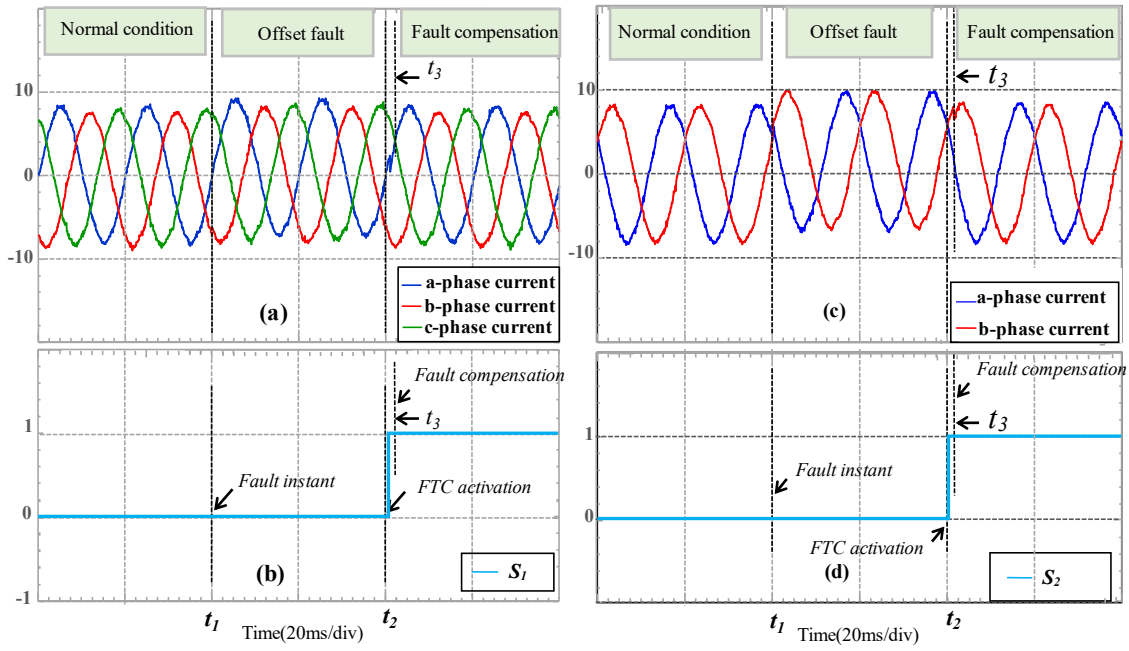

Figure 9 Experimental results for single-phase and double-phase offset fault in measurement current circuit **(a)** grid current **(b)** signal S_1. Experimental results for offset fault: **(c)** grid current **(d)** alarm signal S_2.

Table 2 Comparison study of FTC strategy

FTC Strategy	Numbers of phase	Tolerance Time	Whether it improve the diagnosis accuracy
Space vector decomposition [12]	Multiple	10ms	No
Signal reconstitution [15]	single	40ms	No
Independent observer [13]	single and double	8 ms	No
Proposed strategy	single and double	2ms	Yes

V. Analysis And Limitations of The FTC Method

To further assess the effectiveness of the proposed fault detection and compensation strategy, simulation outcomes were directly compared with experimental measurements under various single-phase and double-phase DC offset fault scenarios. The comparison reveals a high level of consistency between the simulated and experimental results, as both residual signals and alarm indicators reliably identify the faulty phases. In the case of single-phase faults, the S1 indicator correctly detects the affected phase, and the corresponding compensation restores the measured current to its accurate value within approximately 2ms. Similarly, for double-phase faults, the S2 indicator successfully pinpoints the faulty phase pair, while the compensation signals quickly correct the distorted measurements. These findings confirm the method's robustness and suitability for real-time application in practical grid-connected inverter systems.

The proposed fault-tolerant control scheme demonstrates significant advantages in detecting and correcting DC offset faults in one or two phases, providing faster response times and higher diagnostic accuracy compared to conventional techniques. Table 1 summarizes the performance comparison between the proposed approach and existing state-of-the-art methods, highlighting the reduced fault-tolerance duration and improved fault detection precision. Despite these strengths, certain limitations remain. Specifically, when identical DC offset faults occur simultaneously across all three phases, the method cannot detect them due to the cancellation of common-mode components during the coordinate transformation, which renders the residual signals ineffective. Addressing this limitation will be a focus of future research, with the aim of developing complementary strategies capable of identifying such common-mode faults and enhancing overall system reliability. Additionally, in cases where the current controller operates with a very high bandwidth, it may inadvertently mask DC offset faults by adjusting the voltage reference, potentially reducing detection effectiveness. However, in most practical scenarios, controller bandwidth is constrained, allowing residual signals to remain sufficiently indicative of offset faults. Furthermore, the method operates without additional hardware, shows intrinsic resilience to high-frequency noise due to its reliance on low-frequency synchronous-frame components, and provides a solid foundation for further extensions to handle real-world uncertainties such as sensor disturbances, grid frequency variations, and long-term offset drifts.

VI. Conclusion

This paper introduces a FTC strategy to address offset faults in the current measurement circuits of GCIs. The approach focuses on analyzing unwanted AC ripple currents in the d-axis at the grid's fundamental frequency. A band-pass filter is employed to extract these ripple currents, which are then used to detect, isolate, and compensate for DC offset faults in both single-phase and two-phase current measurements. The fault detection, isolation, and compensation algorithm helps the system quickly recover optimal performance without requiring additional hardware. Experimental results demonstrate that the method swiftly restores the system to normal operation under various fault conditions, with no changes to the control system.

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